

METHODS AND CIRCUITS FOR
PROGRAMMABLE AUTOMATIC BURST MODE CONTROL
USING AVERAGE OUTPUT CURRENT

Field of the Invention

5 **[0001]** The present invention relates to power
converter circuits. More particularly, the present
invention relates to methods and circuits for power
converters that automatically transition into and out
of a low power consumption mode based on load current.

10

Background of the Invention

[0002] Voltage regulators, also known as power
converters, provide a regulated output voltage from a
voltage source that may be poorly-specified or
15 fluctuating, or that may be at an inappropriate
amplitude for the load. Such regulators may employ a
switching circuit that includes one or more switching
elements coupled in series or in parallel with the
load. The switching elements may be, for example,
20 power metal-oxide semiconductor field-effect transistor
(MOSFET) switches.

[0003] Control circuitry regulates the output
voltage and the current supplied to the load by cycling

the switch circuit between ON and OFF states. The duty cycle of the switch circuit controls the flow of power to the load, and can be varied by a variety of methods. For example, the duty cycle can be varied by (1) fixing
5 the pulse stream frequency and varying the ON or OFF time of each pulse, (2) fixing the ON or OFF time of each pulse and varying the pulse stream frequency, or (3) a combination thereof.

[0004] To vary the ON or OFF time of each pulse or
10 the pulse stream frequency, the control circuitry may monitor the regulator's output voltage and generate a feedback signal V_e that is proportional to the difference between the regulator's output voltage and the regulated voltage. V_e may be used to provide either
15 "voltage-mode" or "current-mode" regulation. In voltage-mode regulation, V_e and a periodic sawtooth waveform V_s may be provided as inputs to a comparator, the output of which controls the duty cycle of the switch circuit. In current-mode regulation, a voltage
20 V_i may be generated that is proportional to the current in the output inductor, and V_i and V_e may be provided as inputs to a comparator, the output of which controls the duty cycle of the switch circuit.

[0005] Synchronous switching regulators include at
25 least two switching elements that typically are driven by non-overlapping drive signals to supply current at a regulated voltage to a load. Synchronous switching regulators that use power MOSFET switches frequently are used in portable battery-powered electronic
30 products and thermally-sensitive products. These regulators convert the typically fluctuating input voltage to a regulated output voltage. Such regulators

provide high operating efficiency and thus long battery life with little heat generation.

[0006] One problem with switching regulators is that the efficiency of the regulator decreases as the load current is reduced to low levels due to switching and quiescent losses. This is particularly problematic in battery-powered applications, which may spend much of their operating time in a low power draw mode (i.e., when load current demand is low).

10 [0007] To maintain high efficiency at light load, thereby increasing battery life, switching power converters may transition from a NORMAL operating mode, e.g., a fixed frequency pulse-width modulation (PWM) mode of operation, to a low power consumption mode in which switching and quiescent losses are significantly reduced. One example of a low power consumption mode is a BURST mode operation, which sometimes also is referred to as a type of pulse frequency modulation with intermittent bursts of pulses. In BURST mode, the voltage regulator operates sufficiently long to bring the output voltage into regulation, after which the converter transitions into SLEEP mode. In SLEEP mode, all switching stops and all the active switching elements are maintained OFF for a period of time that varies as a function of load current, the quiescent current of the converter is reduced, and the load is supported by energy stored in an output capacitor. During SLEEP, additional components of the power converter can be but need not be turned OFF. When the output voltage decreases below a threshold level, e.g., 1% below the regulated value, the converter "awakens" from SLEEP mode and resumes switching until the output voltage again is within regulation limits, at which

point the converter resumes SLEEP mode. Alternatively, some switching power converters may transition directly from NORMAL operation to SLEEP mode, maintaining all active switching elements OFF and reducing quiescent
5 current to reduce power consumption. In this manner, high efficiency can be maintained over a wide range of load current since the time spent in SLEEP mode increases as the load current demand is reduced.

[0008] When the power converter is subjected to
10 heavier loads, however, NORMAL operating mode, in which the converter switch continuously alternates between an ON state and an OFF state to maintain the output voltage at the regulated level, may be more beneficial than BURST mode operation. Accordingly, the converter
15 may be configured for transition between NORMAL operating mode and BURST mode as the load varies.

[0009] Some applications may be able to provide a mode control signal, giving the converter "advance warning" of an impending increase or decrease in load.
20 There are other applications in which a user cannot provide this control, and the converter must be able to switch between modes automatically, based on load, while maintaining regulation.

[0010] Preferably, a burst mode control circuit
25 would have means of sensing average load current and switch between modes automatically based on a user-programmed current threshold. It would also respond quickly to sudden load changes, and easily be controlled by the host for manual operation, while
30 requiring a minimum number of components.

[0011] There are a number of existing methods for implementing automatic mode control (see, e.g., U.S. Patent No. 5,481,178 to Wilcox et al.). One method

used by current mode converters is to sense load current by monitoring output voltage from a feedback error amplifier. When this voltage drops below a predetermined level, indicating a certain peak inductor
5 current, the converter goes into SLEEP mode. The converter comes out of the SLEEP mode when the output voltage has dropped below a pre-defined threshold. Thereafter, the converter wakes up and resumes switching. The major problem with this method is that
10 the error voltage is an indication of peak inductor current, not average load current. This may cause the mode transition point to vary as much as 10:1, as a function of the V_{IN}/V_{OUT} ratio, inductance, and switching frequency. It also is restricted to converters using
15 current mode control.

[0012] Another method is described in the datasheet for Unitrode's UC1874 buck regulator. The UC1874 employs fixed frequency average current mode control and improves light load efficiency with a programmable
20 standby mode during which the MOSFET drivers and the oscillator are disabled. The UC1874 senses average output current by monitoring voltage from a feedback error amplifier. When that voltage, which is indicative of the average output current, drops below a
25 programmable voltage threshold, the converter transitions into the standby mode. One problem with the UC1874 is that the output signal from the error amplifier is accurate only during steady state conditions. During transient conditions, the output
30 voltage from the error amplifier may not be an accurate indication of the average output current due to potential lags in responsiveness that result from employment of average current-mode control.

[0013] Another mode control method and circuit is based on the sensing of discontinuous inductor current as an indication of light load. This circuit is not easily programmable, and is subject to large mode
5 threshold variation with V_{IN} , V_{OUT} , inductance, and switching frequency. Furthermore, such a circuit also may require a larger, more expensive inductor having a greater inductance to achieve the desired load transition threshold.

10 [0014] In view of the foregoing, it would be desirable to provide methods and circuits for controlling a voltage regulator having a smooth and repeatable transition between operating modes.

[0015] It also would be desirable to provide methods
15 and circuits for automatic transition of a voltage regulator into and out of a low power consumption mode at a mode transition point or threshold that can be set independently of input voltage, output voltage, inductance, and switching frequency.

20 [0016] It further would be desirable to provide methods and circuits for automatic transition of a voltage regulator into and out of a low power consumption mode in which the mode transition point or threshold is easily programmable.

25 [0017] It even further would be desirable to provide methods and circuits for automatic transition of a voltage regulator into and out of a low power consumption mode that may be used in conjunction with voltage mode or current mode control to vary the duty
30 cycle of a switch.

[0018] In addition, it would be desirable to provide methods and circuits for transition between operating modes by manual override.

Summary of the Invention

[0019] In view of the foregoing, it is an object of the present invention to provide methods and circuits
5 for controlling a voltage regulator having a smooth and repeatable transition between operating modes.

[0020] It also is an object of the present invention to provide methods and circuits for automatic transition of a voltage regulator into and out of a low
10 power consumption mode at a mode transition point or threshold that can be set independently of input voltage, output voltage, inductance, and switching frequency.

[0021] It further is an object of the present
15 invention to provide methods and circuits for automatic transition of a voltage regulator into and out of a low power consumption mode in which the mode transition point or threshold is easily programmable.

[0022] It even further is an object of the present
20 invention to provide methods and circuits for automatic transition of a voltage regulator into and out of a low power consumption mode that may be used in conjunction with voltage mode or current mode control to vary the duty cycle of a switch.

25 [0023] In addition, it is an object of the present invention to provide methods and circuits for transition between operating modes by manual override.

[0024] These and other objects of the present
invention are accomplished by providing methods and
30 circuits that automatically transition a power converter into and out of a low power consumption mode based on load current demand by monitoring output current and averaging the monitored output current to

develop a signal indicative of average output current. In one embodiment, a synchronous switching regulator is provided having a circuit that monitors and averages the regulator's output current, creating a voltage
5 signal indicative of the average output current. When the indicative voltage is greater than a user-programmable mode transition threshold, indicating a high load current demand, the voltage regulator commands a NORMAL operating mode (e.g., fixed frequency
10 mode) in which the output voltage is maintained at the regulated level by continuously adjusting inductor current I_L . When the indicative voltage is less than the user-programmable mode transition threshold, indicating a low load current demand, the voltage
15 regulator commands BURST mode. A user may easily program the average output current, and thereby the load current demand, at which mode transition occurs by selection of a resistor. Advantageously, the methods and circuits of the present invention permits the duty
20 cycle of the voltage regulator to be controlled using either current mode or voltage mode control.

[0025] Embodiments also may be configured to permit a user to override the automatic mode transition and manually or digitally control transition into and out
25 of BURST mode.

Brief Description of the Drawings

[0026] Further features of the present invention, its nature and various advantages will be more apparent
30 from the accompanying drawings and the following detailed description, in which:

[0027] FIG. 1A is a simplified block diagram of an embodiment of the present invention for automatically

transitioning a power converter into and out of BURST mode;

[0028] FIG. 1B is a partial block diagram of a circuit that permits a user to manually control
5 transition of a voltage regulator into and out of BURST mode;

[0029] FIG. 2 is a block diagram of a synchronous step-down voltage regulator incorporating the automatic BURST control circuit of FIG. 1A, a feedback amplifier,
10 and features for improved transient response;

[0030] FIG. 3A is a block diagram of a synchronous 4-phase boost voltage regulator employing an embodiment of the automatic BURST mode control circuit of the present invention;

15 [0031] FIG. 3B is a graph of output ripple current with single and 4-phase boost regulation;

[0032] FIGS. 3C-E show illustrative current and voltage waveforms of the voltage regulator of FIG. 3A;

[0033] FIGS. 4A-4C are partial block diagrams of
20 alternative circuits to transition the voltage regulators of FIGS. 1, 2, and/or 3A into BURST and/or SLEEP modes;

[0034] FIG. 4D is a partial block diagram showing how the voltage regulator of FIG. 3A is configured to
25 deactivate three of four phases during BURST mode;

[0035] FIG. 4E is an illustrative schematic diagram of a current mirror for use with the circuit of the present invention; and

[0036] FIG. 5 is a simplified block diagram of a
30 synchronous boost voltage regulator employing the automatic BURST mode control circuit of the present invention.

Detailed Description of the Invention

[0037] To increase the efficiency of a power converter, the present invention comprises methods and circuits that may be integrated into the power converter circuit to automatically transition the power converter into BURST mode when load current demand is low and out of BURST mode when the load current demand is high. The present invention, an illustrative embodiment of which is shown in FIG. 1A, transitions power converter control circuit 10 into and out of BURST mode responsive to load current demand by monitoring output current (I_{OUT}) and developing a signal indicative of an average of the monitored output current ($I_{OUT,AVG}$).

[0038] In particular, power converter control circuit 10 regulates the output voltage V_{OUT} by controlling the converter output current such that the average output current supplied to output capacitor C_{OUT} is sufficient to support the current drawn from the output capacitor by the load at an output voltage V_{OUT} within a desired range of a nominal regulated value. When load current demand is low, average output current $I_{OUT,AVG}$ also is low. Likewise, when load current demand is high, so too is the average output current. Accordingly, BURST mode control circuit 12 of the present invention senses low load current demand by sensing low average output current.

[0039] In the embodiment of the present invention illustrated in FIG. 1A, BURST mode control circuit 12 includes current mirror 14 that monitors output current I_{OUT} and generates a current proportional to output current I_{OUT} . The current (I_{OUT}/K) generated by the current mirror, an illustrative embodiment of which is

provided in greater detail hereinbelow, may be a small fraction of the output current. Because output current I_{OUT} comprises a pulsed current that is a function of the switching frequency of converter control circuit 10, V_{OUT} , V_{IN} , and the inductance of an inductor of the power converter, mirrored current I_M also is pulsed in nature. Mirrored current I_M is fed to user-programmable filter 15 having programming resistor 16 (R_{BURST}) and filtering capacitor 18, the capacitance of which is selected to filter the pulses of mirrored current I_M and reduce the ripple of the voltage that is generated across resistor 16 and capacitor 18. That voltage (V_{BURST}) is indicative of average output current $I_{OUT,AVG}$ and used to transition the power converter automatically into and out of BURST mode.

[0040] In particular, V_{BURST} is fed into the inverting input of hysteretic comparator 20 and compared to a reference voltage that is fed into the non-inverting input of hysteretic comparator 20. When V_{BURST} falls below a first user-programmable mode transition threshold, indicating a light load current demand, hysteretic comparator 20 outputs a signal HIGH that commands converter control circuit 10 to operate in BURST mode. Hysteresis of comparator 20 prevents oscillation between modes due to ripple voltage on capacitor 18. The capacitance of capacitor 18 preferably is selected to reduce ripple to less than the hysteresis of comparator 20. When V_{BURST} increases beyond a second, higher user-programmable mode transition threshold, indicating a heavy load current demand, hysteretic comparator 20 outputs a signal LOW that is fed back to power converter control circuit 10 to transition out of BURST mode and command NORMAL

operation of the converter. Illustrative NORMAL operational modes include fixed frequency or variable frequency operation with continuous or discontinuous current, e.g., as described with respect to the voltage converter of FIG. 1 of U.S. Patent No. 5,481,178 to Wilcox et al. As used herein, the term "user-programmable" refers to the capability of varying parameters of the power converter with external components.

10 **[0041]** In accordance with one aspect of the present invention, a user may program power converter control circuit 10 to transition into and out of BURST mode at a desired average output current by a calculated or empirical selection of an appropriate value for the resistance of programming resistor 16. In particular, programming resistor 16 (R_{BURST}) may be selected based on the following equation:

$$R_{BURST} = K * V_{REF} / I_{BURST}$$

where K is the mirror ratio I_{OUT}/I_M , V_{REF} is the reference voltage at the non-inverting input of hysteretic comparator 20, and I_{BURST} approximately is the average output current and, and thus the load current, at which the power converter transitions into and out of BURST mode, neglecting the small voltage ripple across capacitor 18 and the hysteresis of comparator 20.

25 **[0042]** For example, if K is 2000:1, V_{REF} is 1.0V, and R_{BURST} is 10k Ω , power converter control circuit 10 transitions into and out of BURST mode at an average output current of approximately 200mA, neglecting the small voltage ripple across capacitor 18 and the hysteresis of comparator 20. Accordingly, for load current demands greater than approximately 200mA, BURST mode control circuit 12 would command converter control

circuit 10 to operate in NORMAL mode. However, when the load current demand decreases to less than approximately 200mA, BURST mode control circuit 12 would automatically transition converter control circuit 10 to BURST mode operation. Of course, one of ordinary skill in the art would appreciate that the current ratio, reference voltage and resistance values may be modified based on design choice.

[0043] Advantageously, the design of the present invention permits a user to easily program the mode transition point independently of input voltage V_{IN} , output voltage V_{OUT} , inductance, or switching frequency. Furthermore, the high-efficiency circuit of the present invention may be integrated with any converter topology (e.g., buck, boost, inverter, or combinations thereof) and used with either current or voltage mode control.

[0044] Programming resistor 16 and filtering capacitor 18 may be replaced by other known user-programmable filter circuits that average the pulsed nature of mirrored current I_M to generate an output signal that may be employed by hysteretic BURST comparator 20 to automatically transition power converter control circuit 10 into and out of BURST mode. The mode transition control circuit of FIG. 1A also may be used to transition the power converter into SLEEP mode directly from NORMAL operating mode and out of SLEEP mode directly into NORMAL operating mode.

[0045] In accordance with another aspect of the present invention, BURST mode control circuit 12 may be configured to permit manual transition of the voltage regulator into and out of BURST mode. More specifically, a user may force circuit 12 to operate in BURST mode by sinking the BURST PIN to ground or to

operate in NORMAL mode by pulling the BURST PIN up to a voltage greater than V_{REF} (but preferably no greater than V_{OUT}). To facilitate manual transition, user-actuable switch 22 optionally may be provided, as illustrated in FIG. 1B. For example, switch 22 may be coupled to ground in a first position and coupled to V_{OUT} in a second position. Switch 22 may comprise an optional third position in which the switch may be coupled to programming resistor 16 and filtering capacitor 18 to enable automatic transition into and out of BURST mode. Alternatively, switch 22 also may comprise a digitally programmable switch.

[0046] FIG. 2 illustrates the automatic BURST mode control circuit of FIG. 1A integrated with a synchronous step-down power converter using current-mode control, including a feedback error amplifier and features for improved transient response. The voltage regulator of FIG. 2A may be used to provide a regulated DC output voltage V_{OUT} at terminal 24 for driving load 26, which, e.g., may be a portable laptop computer or other battery-operated system. The voltage regulator operates from a supply voltage V_{IN} , e.g., a battery, coupled to terminal 28. When hysteretic BURST comparator 20 determines that the voltage at the BURST pin (V_{BURST}), which is indicative of the average output current and the load current demand, is greater than a mode transition threshold programmed by programming resistor 16 and offset by the hysteresis of BURST comparator 20, the BURST comparator outputs a logic LOW, commanding the power converter to operate in its NORMAL mode.

[0047] When the power converter of FIG. 2 is in NORMAL operational mode, output voltage V_{OUT} may be

maintained approximately at a regulated level by continuously and synchronously switching active switch elements 30 and 32, e.g., MOSFETs, of push-pull switch 34 to adjust the duty cycle of the switch. Push-pull switch 34 supplies current to energy storage elements inductor 36 (L_1) and output capacitor 38 (C_{OUT}), which together smooth the alternating supply of current so that load 26 is provided a regulated voltage.

[0048] MOSFETs 30 and 32 respectively are driven by drivers 40 and 42, which in turn are controlled by one-shot circuit 44. One-shot circuit 44 provides an OFF pulse of constant duration during which time MOSFET 30 is held OFF and MOSFET 32 is held ON, causing inductor current I_L to decrease. At the termination of the OFF pulse, one-shot circuit 44 provides an ON pulse during which time MOSFET 30 is held ON and MOSFET 32 is held OFF, causing the inductor current to increase.

Accordingly, one-shot circuit 44 alternately turns active switch elements 30 and 32 ON and OFF to provide an alternating supply of current to inductor 36 and output capacitor 38.

[0049] The duty cycle of one-shot circuit 44 is controlled by current comparator 46, which compares a feedback voltage V_{FB} that is proportional to output voltage V_{OUT} with a voltage representative of inductor current I_L . Resistor divider 48A/48B (R_1/R_2 respectively) divides output voltage V_{OUT} to generate feedback voltage V_{FB} . Inductor current I_L is monitored by differential amplifier 50 disposed across resistor 52, which in turn is disposed in series with inductor 36.

[0050] In NORMAL mode, the voltage regulator of FIG. 2 controls inductor current I_L so that feedback voltage

V_{FB} is regulated to be substantially equal to a reference voltage, which in turn regulates output voltage V_{OUT} . More specifically, error amplifier 54 is used to compare feedback voltage V_{FB} to a reference voltage V_{REF} . When one-shot circuit 44 provides an ON pulse, MOSFET 30 is turned ON and inductor current I_L ramps up at a rate dependent on $V_{IN}-V_{OUT}$. When I_L ramps up to a threshold level set by output 54A of error amplifier 54, comparator 46 trips and triggers one-shot circuit 44 to provide an OFF pulse of constant duration, during which MOSFET 30 is turned OFF and MOSFET 32 is turned ON. This in turn causes inductor current I_L to ramp down at a rate dependent on V_{OUT} . Once the OFF pulse provided by one-shot circuit 44 times out, MOSFET 30 turns ON and MOSFET 32 turns OFF, again causing inductor current I_L to ramp up and the cycle to repeat.

[0051] Accordingly, the power converter of FIG. 2 comprises a first control circuit that continuously adjusts current flowing through inductor 36 in a NORMAL operational mode. In the embodiment of FIG. 2, the first control circuit illustratively comprises error amplifier 54, comparator 46, one-shot 44, resistor 52 and differential amplifier 50. Of course, one of ordinary skill in the art would appreciate that other control circuits also may be employed based on design choice.

[0052] In accordance with the present invention, when hysteretic BURST comparator 20 determines that the average output current, and thus the load current demand, has decreased below the current level that corresponds to the mode transition threshold set by programming resistor 16 and offset by the hysteresis of

BURST comparator 20, the BURST comparator outputs a logic HIGH, and the power converter transitions into BURST mode. While in BURST mode, feedback error amplifier 54 operates as a SLEEP comparator to
5 transition the voltage converter into and out of SLEEP mode responsive to output voltage V_{OUT} . When SLEEP comparator 54 determines that output voltage V_{OUT} is greater than a SLEEP threshold, e.g., 1% greater than the desired regulated voltage level, comparator 54
10 outputs a logic LOW.

[0053] That signal is inverted by inverter 55 and combined with the logic HIGH signal output by BURST comparator 20 to cause AND gate 56 to command transition of the voltage regulator into SLEEP mode,
15 during which the switching transistors of the power converter are kept OFF. To further reduce power consumption during SLEEP and/or BURST mode, and thereby increase efficiency, the regulator circuit can be but need not be configured to turn OFF other circuit
20 components which are not needed while the regulator is in SLEEP and/or BURST mode. During SLEEP mode, energy stored in output capacitor 38 maintains output voltage V_{OUT} substantially at the regulated voltage and supports load current demand.

[0054] When SLEEP comparator 54 determines that
25 output voltage V_{OUT} is less than a WAKE threshold, e.g., 1% less than the desired regulated voltage level, comparator 54 trips and outputs a logic HIGH signal that wakes up the converter to start a new BURST cycle
30 and recharge output capacitor 38 in BURST mode until SLEEP comparator 54 again outputs logic LOW. To recharge output capacitor 38, the power converter may be configured to alternately turning switch transistors

30 and 32 ON and OFF so as to vary the duty cycle. Alternatively, the power converter may be configured to maintain P-MOSFET 30 ON and maintain N-MOSFET 32 OFF

[0055] When SLEEP comparator 54 again determines
5 that output voltage V_{OUT} is greater than the SLEEP threshold, SLEEP comparator 54 outputs a logic LOW that puts the circuit back in SLEEP mode. The rate at which the regulator "wakes up" to recharge output capacitor C_{OUT} automatically adapts to the load current demand.
10 The above-described procedure of waking up the converter and returning the power converter to sleep after recharging the capacitor is repeated as long as the load current demand is below the current threshold that corresponds to the user-programmable mode
15 transition threshold.

[0056] When hysteretic BURST comparator 20 determines that the voltage at the BURST pin (V_{BURST}), which is indicative of the average output current and the load current demand, is greater than the user-
20 programmable mode transition threshold, BURST comparator 20 outputs a logic LOW, which transitions the voltage regulator out of BURST mode into NORMAL operation. Since the BURST mode signal feeding into AND gate 56 now is at a logic LOW, AND gate 56 may no
25 longer command the converter to enter SLEEP mode regardless of the output of SLEEP comparator 54, which now reverts to function as an error amplifier.

[0057] Accordingly, the power converter of FIG. 2 comprises a second control circuit that transitions the
30 power converter from a NORMAL operational mode into a low power consumption mode, e.g., BURST or SLEEP. In the embodiment of FIG. 2, the second control circuit illustratively comprises current mirror 14 and

hysteretic comparator 20, which accepts a signal generated by filter 15 that provides an indication of the average output current. If the low power consumption mode is a BURST mode, the second control
5 circuit additionally may comprise, for example, SLEEP comparator 54, which also is employed in the NORMAL mode as error amplifier 54, inverter 55 and AND gate 56 to command the active switching elements to be maintained OFF during at least part of the low power
10 consumption mode.

[0058] Advantageously, the mode transition point of the voltage regulator of the present invention is not subject to considerable variation, and therefore is repeatable. This is due to the fact that the automatic
15 burst mode control circuit of the present invention is responsive to the average output current directly and not the output voltage, which (in a current mode control circuit) could cause the mode transition point to vary as much as 10:1 as a function of input and
20 output voltage, inductance, switching frequency and noise. Furthermore, since the burst mode control circuit of the present invention directly monitors output current and averages the monitored output current to generate a signal indicative of the average
25 thereof, the present burst mode control circuit responds quickly and accurately to changes in load current demand even during transient conditions.

[0059] It will be apparent to one of ordinary skill in the relevant art that one-shot constant OFF-time
30 circuit 44 may be replaced with a pulse-width modulator circuit either of the type well-known in the art or otherwise, the pulse-width modulator circuit providing a pulse-width modulated signal in response to a control

signal. Alternatively, one-shot constant OFF-time circuit 44 also may be replaced with a one-shot constant ON-time circuit or a variable OFF-time circuit that provides a variable OFF-time control signal dependent on, e.g., output voltage V_{OUT} and input voltage V_{IN} . U.S. Patent Serial No. 5,481,178 to Wilcox et al. describes one example of such a variable OFF-time circuit that may be used to reduce the generation and emission of audible noise from inductor 36 at low input voltages. Alternatively, the voltage regulator of FIG. 2 also may be configured to turn MOSFET 30 ON and MOSFET 32 OFF when the signal from differential amplifier 50 is less than a first threshold set relative to the output signal from error amplifier 54, and turn MOSFET 30 OFF and MOSFET 32 ON when the signal from differential amplifier 50 is greater than a second threshold (lower than the first threshold) also set relative to the output signal from error amplifier 54. A comparator with hysteresis could be used for this purpose.

[0060] FIG. 2 also incorporates additional optional features for improved transient response. For example, to provide faster response to a sudden increase in load current demand that reduces output voltage V_{OUT} below an under-voltage mode transition threshold, e.g., 3-4% below the desired regulated output voltage, when the voltage regulator is operating in low power consumption mode, e.g., BURST mode, under-voltage comparator 58 trips and commands an immediate transition from BURST mode to NORMAL operating mode in a manner described in greater detail below. To prevent premature transition back to BURST mode, e.g., due to a slight overshoot in output voltage V_{OUT} , voltage source 60 quickly recharges

filtering capacitor 18 back to a voltage that is greater than the mode transition threshold set by programming resistor 16. Advantageously, rather than wait for mirrored current I_M to recharge filtering capacitor 18 above the mode transition threshold, this provides a faster response to a sudden increase in load current demand. When output voltage V_{OUT} is recharged back to regulation level under NORMAL operating mode, under-voltage comparator 58 may revert to a logic LOW. Until the average output current again reduces to a current level less than the threshold programmed by programming resistor 16, the converter remains in NORMAL operating mode. Voltage source 60 may be coupled to input voltage V_{IN} and/or output voltage V_{OUT} . In one embodiment, voltage source 60 may charge filtering capacitor 18 to the maximum of input voltage V_{IN} and output voltage V_{OUT} .

[0061] Similarly, if the load current demand exceeds the output current supplied by the power converter during the forced BURST mode operation described above with respect to FIG. 1B, causing output voltage V_{OUT} to reduce below the under-voltage mode transition threshold, e.g., 3-4% below the desired output voltage, under-voltage comparator 58 trips and commands an immediate transition from BURST mode to NORMAL operating mode. Once output voltage V_{OUT} again is in regulation, the voltage regulator will return to BURST mode and the cycle will repeat, resulting in about 3-4% output ripple. Output ripple may be reduced by coupling a small feedforward capacitor across resistor 48A.

[0062] In alternative embodiments, AND gate 73 may accept additional inputs and thereby require additional

conditions to be satisfied before switch 70 is activated to couple voltage source 60 to filtering capacitor 18. For example, as shown in FIG. 2, AND gate 73 also may accept a signal from a soft-start circuit (not shown), requiring that the soft-start time be completed before switch 70 is closed.

[0063] To provide frequency compensation when the converter transitions from BURST mode to NORMAL operation, the converter also may incorporate compensation network 62 having, e.g., compensation resistor 64 in series with compensation capacitor 66. In BURST mode, SLEEP comparator 54 is disconnected from compensation network 62. This improves the converter's response when returning to NORMAL operation by preventing compensation capacitor 66 from discharging during BURST mode. In applications in which the converter may operate in BURST mode for extended periods, compensation network 62 may be clamped by clamp 68 in BURST mode, again preventing compensation capacitor 66 from discharging.

[0064] In operation, when the load current demand is high, hysteretic BURST comparator 20 outputs a logic LOW that commands the converter circuit to operate in a NORMAL mode and switch 70 to disconnect voltage source 60 from charging filtering capacitor 18. The converter then regulates the output voltage and current so that inductor current I_L is regulated at a level required to support the load. When load current demand decreases, however, the duty cycle of switch 34 also decreases responsive thereto. The resulting reduction in the average output current delivered to output capacitor 38 to support the load is reflected in voltage V_{BURST} at the BURST PIN. Once V_{BURST} has decreased to a voltage level

below the first user-programmable mode transition threshold, hysteretic BURST comparator 20 outputs a logic HIGH, which is fed to AND gate 72 along with the inverted output of under-voltage comparator 58.

5 Thereafter, the converter circuit is commanded to operate in BURST mode.

[0065] The logic HIGH output of BURST comparator 20 also is fed to AND gate 73 along with the logic LOW output of under-voltage comparator 58 to maintain
10 disablement of switch 70, and thereby maintain an open connection between voltage source 60 and filtering capacitor 18. As discussed above, under-voltage comparator 58 may revert to a logic LOW when output voltage V_{OUT} is recharged back to the regulated level in
15 NORMAL operating mode.

[0066] In BURST mode, AND gate 72 outputs a logic HIGH signal that opens switch 74 to disconnect compensation network 62 from the remainder of the regulator circuit, and closes switch 76 to connect
20 clamp 68 to compensation network 62 and thereby prevent compensation capacitor 66 from discharging. The logic HIGH signal from AND gate 72 also is fed to AND gate 56, which now may command the regulator circuit to transition into SLEEP mode responsive to output signal
25 54A of SLEEP comparator 54. As described hereinabove, when the converter circuit is in BURST mode and output voltage V_{OUT} is greater than the SLEEP threshold, e.g., 1% above the desired output voltage, SLEEP comparator 54 outputs a logic LOW that commands the converter
30 circuit to operate in SLEEP mode. However, when the converter circuit is in BURST mode and output voltage V_{OUT} decreases to be less than a WAKE threshold, e.g., 1% less than the desired output voltage, SLEEP

comparator 54 outputs a logic HIGH that wakes up the converter to recharge output capacitor 38 until SLEEP comparator 54 again outputs a logic LOW.

[0067] When load current demand suddenly increases, output capacitor 38 may be unable to sustain output voltage V_{OUT} approximately at the regulated level. If output capacitor 38 suddenly and quickly is discharged, output voltage V_{OUT} may decrease at a rate faster than the rate at which filtering capacitor 18 is recharged by mirror current I_M . When output voltage V_{OUT} decreases to a level less than the under-voltage mode transition threshold, e.g., 3-4% below that of the desired output voltage, under-voltage comparator 58 trips and outputs a logic HIGH. This signal then is fed to AND gate 72, which immediately transitions the converter out of BURST mode. The logic HIGH output of the under-voltage comparator also is fed to AND gate 73, which commands switch 70 to close, connecting voltage source 60 to filtering capacitor 18. Voltage source 60 then quickly charges filtering capacitor to a voltage that is greater than the second user-programmable mode transition threshold. This in turn causes the hysteretic comparator to output a logic LOW that opens switch 70, disconnecting voltage source 60 from filtering capacitor 18. Thereafter, the regulator circuit operates in NORMAL operating mode until V_{BURST} once again drops below the programmed mode transition threshold, indicating that the average output current (and thus the load current demand) is low, at which time the above-described cycle repeats.

[0068] In addition to the buck topology described above, the high-efficiency BURST mode control circuit of the present invention also may be integrated with

switching regulators of different topologies. For example, FIG. 3A depicts a block diagram of a multiphase boost regulator circuit. Switching regulator 80 is a synchronous, 4-phase boost converter that controls the duty cycle in the NORMAL operational mode by pulse width modulation (PWM) and, when load current demand is low, operates in BURST mode. The switching regulator operates in 4-phases, which may be equally spaced (i.e., 90° apart). Advantageously, this increases output ripple frequency by a factor of four (see FIG. 3B), reducing output capacitor ripple, and thereby reducing the output capacitance requirement. Multiphase operation also reduces input current ripple so that input current V_{IN} experiences less noise. To facilitate description of switching regulator 80, the four phases hereinafter will be referred to as Phase A, Phase B, Phase C and Phase D. Of course, it will be obvious to one of ordinary skill in the art that power converter 80 may be configured to operate in more or less phases.

[0069] Each phase of switching regulator 80 respectively is associated with one of four power blocks 81, delineated by dashed lines in FIG. 3A. Each power block 81 may include electrical components that control pulse width modulation, slope compensation, and zero current detection. Each power block 81 interacts with the remainder of the regulator, accepting signals that indicate or control, e.g., NORMAL or BURST mode, SLEEP mode, duty cycle, current limit, start-up and soft-start. Each power block also provides output current to output pins 82, which correspond to each phase. The output pins are in turn coupled to output capacitor 84 and load 86.

[0070] Switching regulator 80 is powered by a voltage source, e.g., a battery, coupled to input terminal 88. Each power block 81 is coupled to its respective input pin 90, which in turn is externally coupled to its respective inductor 92, input terminal 88 and common input capacitor 93. To disable any of the phases, the inductor corresponding to that phase may be eliminated. This permits a user to reduce cost and board area in applications that do not require the full power capability of voltage regulator 80, or where peak efficiency may not be as important as cost and size.

[0071] When the power converter of FIG. 3A is in NORMAL operational mode, output voltage V_{OUT} may be maintained at a regulated level by continuously and synchronously switching active switch elements 94 and 96, a pair of which optionally may be disposed within each power block 81 along with anti-cross conduction circuitry. The switching frequency of each pair of active switch elements, e.g., MOSFETs, are established by oscillator 98 and 4-phase divider/generator 100. Oscillator 98 provides an operational frequency, which may be set via a user programmable resistor 102 coupled between R_T pin 104 and ground. An internally trimmed timing capacitor is provided within the integrated circuit. Divider/generator 100 then divides the oscillator frequency by four to generate the four phases, each phase shifted by 90° .

[0072] Oscillator 98 may be synchronized with an external clock applied to SYNCIN pin 106, and configured to provide an output synchronization pulse that is 180° out of phase from the frequency provided to divider/generator 100 to facilitate synchronization of

two voltage regulators. For example, the output synchronization pulse of a first voltage regulator 80 may be provided to SYNCIN pin 106 of a second voltage regulator 80 to create an 8-phase converter, in which
5 the BURST mode control circuits of the voltage regulators may be disabled for some applications by pulling up on the BURST pin. For example, if a user expects the load current demand to dwell approximately at the current level that corresponds to the user-programmable mode transition threshold for a prolonged
10 period of time, then a user may consider disabling the BURST mode control circuits of the voltage regulators.

[0073] The fixed frequency pulses generated by oscillator 98 and 4-phase generator 100 then may be
15 provided to pulse width modulator 108 of each power block 81, the duty cycle of which may be current mode controlled. In one embodiment, a feedback voltage indicative of output voltage V_{OUT} is fed into error amplifier 110, e.g., a transconductance amplifier.
20 Error amplifier 110 compares the feedback voltage to a reference voltage and outputs error signal V_e . Comparator 112 then compares error voltage V_e and optionally a signal indicative of a user-programmable maximum current limit level to a signal indicative of
25 the peak current, which optionally may be slope-compensated. The peak current signal may be obtained from current mirror 114, which is configured to mirror a fraction of the current flowing through N-MOSFET 96 with little or no current loss. The maximum current
30 limit level may be user-programmed by coupling current limit resistor 116 between ground and over-current protection circuit 118, examples of which are well-known to one of ordinary skill in the art. PWM 108

then controls the duty cycle of voltage regulator 80 responsive to the output of comparator 112, turning each pair of P-MOSFET 94 and N-MOSFET 96 ON and OFF as appropriate to adjust inductor current I_L and thereby regulate output voltage V_{OUT} .

[0074] Accordingly, the power converter of FIG. 3A comprises a first control circuit that continuously adjusts current flowing through inductor(s) 92 in a NORMAL operational mode. In the embodiment of FIG. 3A, the first control circuit illustratively may comprise error amplifier 110, comparator 112, PWM 108, and current mirror 114. Of course, one of ordinary skill in the art would appreciate that other control circuits also may be employed based on design choice.

[0075] In accordance with the present invention, switching regulator 80 also includes a BURST mode control circuit to automatically transition regulator 80 into and out of BURST mode. As discussed hereinabove with respect to FIGS. 1 and 2, current mirror 118 monitors a fraction of output current I_{OUT} with little or no current loss. Mirrored current I_M is fed to user-programmable filter 119 having programming resistor 120 (R_{BURST}) and filtering capacitor 122, the capacitance of which is selected to filter the pulses of mirrored current I_M and reduce the ripple of the voltage (V_{BURST}) that is generated across resistor 120 and capacitor 122. The generated BURST voltage (V_{BURST}) is indicative of average output current $I_{OUT,AVG}$ and is used to automatically transition the power converter into and out of BURST mode.

[0076] In particular, like the BURST mode control circuit of FIGS. 1 and 2, burst voltage V_{BURST} is fed into hysteretic comparator 124 and compared to a

reference voltage. When V_{BURST} falls below a first user-programmable mode transition threshold, indicating a light load current demand, hysteretic comparator 124 outputs a signal HIGH that commands converter 80 to
5 operate in BURST mode. When V_{BURST} increases beyond a second higher user-programmable mode transition threshold, indicating a heavy load current demand, hysteretic comparator 124 commands NORMAL operation of the converter. A user may program converter control
10 circuit 80 to transition into and out of BURST mode at particular average output currents by selecting the resistance of programming resistor 120, as described hereinabove.

[0077] As with the converter described with respect
15 to FIG. 2, error amplifier 110 operates as a SLEEP comparator in BURST mode to transition the voltage converter into and out of SLEEP mode responsive to output voltage V_{OUT} . When SLEEP comparator 110
determines that output voltage V_{OUT} is greater than a
20 SLEEP threshold, e.g., 1% greater than the desired regulated voltage level, voltage V_e at the output of comparator 110 is input into AND gate 125 which then commands transition of the voltage regulator into SLEEP
mode if the voltage regulator is in BURST mode. During
25 SLEEP mode, switching transistors 94 and 96 of the power converter are kept OFF. Additional components of the voltage regulator that are not needed during SLEEP mode also may be but need not be turned OFF during
SLEEP mode to increase regulator efficiency. When
30 SLEEP comparator 110 determines that output voltage V_{OUT} is less than a WAKE threshold, e.g., 1% less than the desired regulated voltage level, comparator 110 trips

and wakes up the converter to start a new BURST cycle and recharge output capacitor 84.

[0078] In an optional embodiment, after the SLEEP comparator commands transition out of SLEEP mode, voltage regulator 80 may be configured to delay the transition by a predetermined finite amount of time, e.g., 5 μ s, to permit bias currents to charge the components of the voltage regulator that were turned OFF during SLEEP mode up to a known operational state, i.e., become "smart." After the end of the delay period, MOSFETS 94 and 96 may be enabled for switching.

[0079] To recharge output capacitor 84 during BURST mode, voltage regulator 80 is configured to shut down oscillator 98, and alternately turn MOSFETs ON and OFF so that (1) the ON time of P-MOSFET 94 and the OFF time of N-MOSFET 96 are determined by the time it takes inductor current I_L to reach a peak current limit that is internally fixed independently of current-limit programming resistor 116; and (2) the OFF time of P-MOSFET 94 and the ON time of N-MOSFET 96 are determined by the time it takes inductor current I_L to return to zero. Zero-current detection comparator 140 is used to perceive zero inductor current I_L . When SLEEP comparator 110 again determines that output voltage V_{OUT} is greater than the SLEEP threshold, the SLEEP comparator outputs a logic LOW, returning the power converter to SLEEP mode. Alternatively, voltage converter 80 may be configured to recharge output capacitor 84 by fixed frequency pulse width modulation or by maintaining P-MOSFET 94 ON and N-MOSFET 96 OFF during the entire wake-up period.

[0080] When hysteretic BURST comparator 124 determines that the average output current, and thus

the load current demand, is greater than the mode transition level programmed by programming resistor 120, BURST comparator 124 transitions voltage regulator 80 out of BURST mode into NORMAL operation. Like the
5 converter circuits of FIG. 2, AND gate 125 prevents voltage regulator 80 from entering SLEEP mode during NORMAL operation.

[0081] Accordingly, the power converter of FIG. 3A comprises a second control circuit that transitions the
10 power converter from a NORMAL operational mode into a low power consumption mode, e.g., BURST or SLEEP. In the embodiment of FIG. 3A, the second control circuit illustratively may comprise current mirror 118 and hysteretic comparator 124, which accepts a signal
15 generated by filter 119 that is indicative of the average output current. If the low power consumption mode is a BURST mode, the second control circuit additionally may comprise, for example, SLEEP comparator 110, which also is employed in the NORMAL
20 mode as error amplifier 110, and AND gate 125 to command the active switching elements to be maintained OFF during at least part of the low power consumption mode.

[0082] FIGS. 3C-3E show illustrative current and
25 voltage waveforms of the voltage regulator of FIG. 3A when the voltage regulator is recharging output capacitor 84 during BURST mode. FIG. 3C depicts the pulsed inductor and rectifier current waveform at light load, which is maximum at peak current I_P ; while FIG. 3D
30 illustrates mirrored rectifier current I_M , in which the pulsed rectifier waveform is reduced by mirror ratio K . FIG. 3E shows the filtered voltage at the BURST PIN when the voltage regulator is operating in BURST mode.

[0083] Also as discussed in greater detail with respect to FIG. 2, voltage regulator 80 may include features for improved transient response. More specifically, voltage regulator 80 may include compensation network 128 (e.g., compensation capacitor 130) that may be disconnected from SLEEP comparator 110 during BURST mode to prevent compensation capacitor 130 from discharging to zero, thereby improving the converter's response when returning to NORMAL operation. When the voltage regulator transitions from BURST mode to NORMAL mode, compensation network 128 is recoupled to SLEEP comparator 110. In applications in which the converter may operate in BURST mode for extended periods, compensation network 128 may be clamped in BURST mode, again preventing compensation capacitor 130 from discharging.

[0084] To provide faster response to sudden increases in load current demand when the voltage regulator is operating in automatic or forced BURST mode, under-voltage comparator 132 outputs a signal to logic gates 126 that commands an immediate transition from BURST mode to NORMAL operating mode when output voltage V_{OUT} decreases below an under-voltage mode transition threshold, e.g., 3-4% below regulation level. To prevent premature transition back to BURST mode, e.g., due to a slight overshoot, in output voltage V_{OUT} , voltage regulator 80 may include internal pull-up circuit 134 that quickly recharges filtering capacitor 122 above the programmed mode transition threshold in a manner similar to that described with respect to FIG. 2 hereinabove. Advantageously, rather than waiting for mirrored current I_M to recharge filtering capacitor 122 above the mode transition

threshold, this provides a faster response to a sudden increase in load current demand. When output voltage V_{OUT} is recharged back to regulation level under NORMAL operating mode, under-voltage comparator 132 reverts to
5 a logic LOW.

[0085] In addition to transitioning voltage converter 80 into and out of BURST mode responsive to BURST comparator 124, voltage regulator 80 may be configured to transition between modes responsive to
10 additional conditions. For example, as illustrated in FIG. 4A, additional conditions may include but are not limited to: (1) output voltage V_{OUT} is greater than input voltage V_{IN} by a predetermined voltage; (2) the soft-start time is completed; (3) supply voltage V_{CC} is
15 at an acceptable level; (4) the reference voltage is at an acceptable level; and (5) under-voltage comparator 132 of FIG. 3A is low. If one or more of these conditions are not satisfied or the BURST comparator indicates that load current demand is high, logic gates
20 136 prohibit transition of voltage regulator 80 into BURST mode.

[0086] Likewise, to transition voltage regulator 80 into SLEEP mode, the regulator also may be configured to respond to additional conditions. For example, as
25 depicted in FIG. 4B, when the voltage regulator is in BURST mode and SLEEP comparator 110 indicates that the regulator should enter SLEEP mode, latch 138 delays transition into SLEEP mode until the latch is set. Latch 138 may be set when zero-current detection
30 comparator 140 (see FIG. 3A) perceives that the current through inductor 92 has decayed to zero. Advantageously, this permits reduction of non-synchronous body diode conduction of internal MOSFET

rectifier 94, increasing efficiency over the small number of pulses in each BURST cycle. If inductor current I_L does not decay to zero within a predetermined amount of time, e.g., 5 μ s, after the SLEEP comparator trips, latch 138 may be set by delay circuit 141.

[0087] In FIG. 4C, the voltage regulator enters SLEEP mode only after the following conditions are satisfied: (1) output V_e of SLEEP comparator 110 indicates that V_{OUT} is greater than the SLEEP threshold; (2) the regulator is in BURST mode; (3) output voltage V_{OUT} is greater than input voltage V_{IN} by a predetermined voltage; (4) the voltage regulator has not been commanded to SHUTDOWN; and (5) either inductor current I_L has decayed to zero or a predetermined time has elapsed since the first three criteria have been met.

[0088] Pursuant to another aspect of the present invention, voltage regulator 80 may be configured to activate only one of the four phases, e.g., Phase A, when the regulator is in BURST mode to increase regulator efficiency. FIG. 4D depicts power blocks 81A-D corresponding to Phases A-D. Each power block 81 has a multiplicity of input lines, including MODE input line 142 that accepts a signal indicating whether the voltage regulator is in BURST mode or NORMAL mode and SLEEP input line 144 that accepts a signal indicating whether the voltage regulator is in SLEEP mode.

Voltage regulator 80 is configured so that, when the regulator enters BURST mode, the MODE signal is fed to MODE inputs 142A-D of power blocks 81A-D and to SLEEP inputs 144B-D of power blocks 81B-D. Accordingly, anytime BURST mode is entered, Phase A remains active while Phases B-D are put into SLEEP mode, remaining OFF while voltage regulator 80 is in BURST mode.

[0089] In an optional embodiment, when power converter 80 is commanded to transition back to NORMAL mode, power blocks 81B-D may be brought out of SLEEP mode after a delay by a predetermined finite amount of
5 time to permit the voltage regulator to become "smart" as discussed hereinabove.

[0090] Each power block 81A-D also has a multiplicity of output lines, including I_ZERO output 146 that dispatches the output signal of zero-current
10 detection comparator 140 (see FIG. 3A), which perceives when inductor current I_L has decayed to zero. Voltage regulator 80 may be configured so that only power block 81A outputs the output signal of its zero-current detection comparator since only Phase A is active
15 during BURST mode. I_ZERO outputs 146B-D of power blocks 81B-D may be left open since Phases B-D are inactivate during BURST mode.

[0091] Examples of modifications that may be made to switching regulator 80 include but are not limited to:
20 (1) operation with a single phase; (2) use of other current limit circuitry either known to those of ordinary skill in the art or otherwise; and/or (3) inclusion of a low battery indicator. Additional modifications may be employed based on design choice.

[0092] Referring now to FIG. 4E, an illustrative current mirror is described for use in the present invention to monitor output current I_{OUT} . Current mirror 148 includes power MOSFET 150, e.g., a p-type MOSFET, coupled in parallel to rectifying MOSFET 94 of
30 the boost converter of FIG. 3A. Mirror MOSFET 150 is coupled to rectifying MOSFET 94 such that well 152, source 154 and gate 156 are respectively connected to the well, switch node, and gate of the rectifying

MOSFET. To replicate the conditions under which rectifying MOSFET 94 operates, drain 158 of mirror MOSFET 150 is maintained at output voltage V_{OUT} . Mirror current I_M is drawn from drain 158 of mirror MOSFET 150.

5 The mirror MOSFET samples a fraction of the current flowing through the rectifying MOSFET, with little or no current loss and thus little impact on regulator efficiency.

[0093] Current mirror 148 also may comprise additional embodiments of current mirrors well-known to those of ordinary skill in the art, e.g., BJT current mirrors, cascode configuration mirrors, Wilson configuration mirrors, modified Wilson configuration mirrors, resistors, etc.

10

[0094] Current mirror 148 also may be employed to monitor current flowing through N-MOSFET 96 of FIG. 3A. In one embodiment, current mirror 148 may include power MOSFET 150, e.g., a n-type MOSFET, coupled in parallel to MOSFET 96. Mirror MOSFET 150 may be coupled to MOSFET 96 such that well 152, source 154 and gate 156 are respectively connected to the well, switch node, and gate of MOSFET 96. To replicate the conditions under which MOSFET 96 operates, drain 158 of mirror MOSFET 150 may be maintained at ground. Mirror current I_M may be drawn from drain 158 of mirror MOSFET 150.

15
20
25

[0095] Referring now to FIG. 5, a simplified schematic diagram of a boost converter incorporating the programmable, automatic BURST control circuit of the present invention is described, in which the dashed lines represent the boundaries of an illustrative monolithic converter integrated circuit (IC). In one embodiment, IC 160 integrally may comprise P- and N-MOSFETs 162 and 164, the duty cycle of which is

30

modulated by modulator 166 and error amplifier 168. Of course, monolithic IC 160 also may be manufactured without integral MOSFETs 162 and 164, which may be coupled to the IC via additional pins.

5 **[0096]** With the exception of programming resistor 170 and filtering capacitor 172, both of which may be selected by the user and coupled to BURST pin 174 external to IC 160, any remaining components 176 of the automatic BURST mode control circuit described with
10 respect to FIGS. 1, 2, 3A, and 4A-4e also may be integrated within IC 160. Compensation network 178 and inductor 180 also may be coupled externally to IC 160 via COMP pin 182 and input pin 184, respectively, so that users may select the resistor, capacitor, and
15 inductor appropriate for their particular applications.

[0097] If monolithic IC 160 is a constant output voltage regulator, voltage divider 186A/186B may be integrated within IC 160. However, if monolithic IC
20 160 is a programmable output voltage regulator, voltage divider 186A/186B may be coupled to monolithic IC 160 externally via FB pin 188.

[0098] As used herein, the term "monitor" and derivatives thereof refer to the action of detecting or measuring the instantaneous value of a current or
25 voltage signal or a fraction thereof. In contrast, the term "sense" and derivatives thereof broadly refer to the action of obtaining some indication, either directly or indirectly, of a current or voltage signal. Furthermore, the term "an output voltage" does not
30 necessarily mean that the voltage at the output of the power converter is a constant value. Rather, as is understood in the art, the power converter's output voltage may vary to some extent.

[0099] Although illustrative embodiments of the present invention are described above, it will be apparent to one skilled in the art that various changes and modifications may be made without departing from the invention. For example, while the above-described figures depict a resistive current shunt and transistor-based current mirror to monitor output current I_{OUT} , additional embodiments of current monitors also may be employed, such as current transformers, Hall effect devices, or optical current sensors.

[0100] In addition, while the above-described embodiments depict the use of synchronous switches, each having two active switching elements that are driven out of phase to supply current at an output voltage to a load, one of ordinary skill in the relevant art would appreciate that either of the two MOSFETs may be replaced with a passive switch element, e.g., a switching diode. The present invention also may be integrated with voltage regulators employing other types of switches having, e.g., a pair of N-MOSFETs, a pair of P-MOSFETs, or bipolar junction transistors.

[0101] It will be apparent to one of ordinary skill in the art that the switching regulators of the present invention could be taken out of SLEEP mode a predetermined time period after going into SLEEP mode, rather than transitioning out of SLEEP mode after load current demand increases as described hereinabove. All reference voltages defining the thresholds may comprise the same threshold levels or one or more different levels, and may be constant or variable in nature.

[0102] Furthermore, while the above-described embodiments incorporate current-mode regulation of the

converter's duty cycle, it should be obvious to one of ordinary skill in the art that the BURST mode control circuit of the present invention also may be integrated with power converters having voltage-mode regulation.

5 Furthermore, the BURST mode control circuit of the present invention also may be integrated with current regulators in a manner similar to that described above.

[0103] It is intended in the appended claims to cover all such changes and modifications that fall
10 within the true spirit and scope of the invention.